

FIG. 1

PRIOR ART

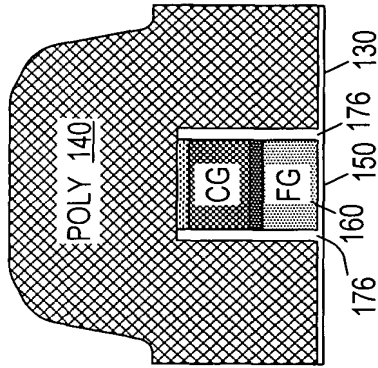


FIG. 2

PRIOR ART

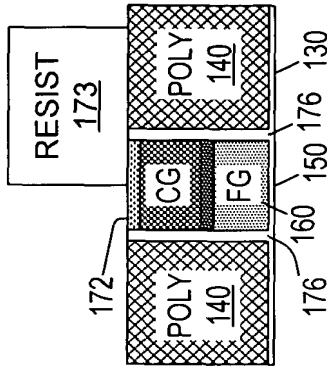


FIG. 3

PRIOR ART

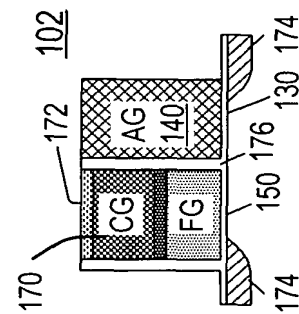


FIG. 4

PRIOR ART

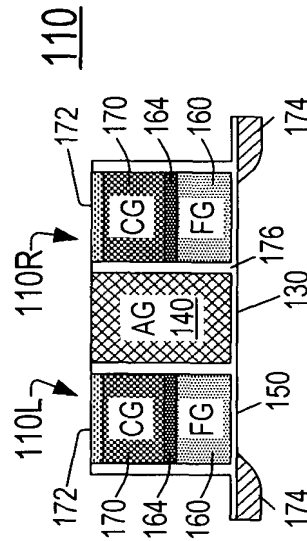
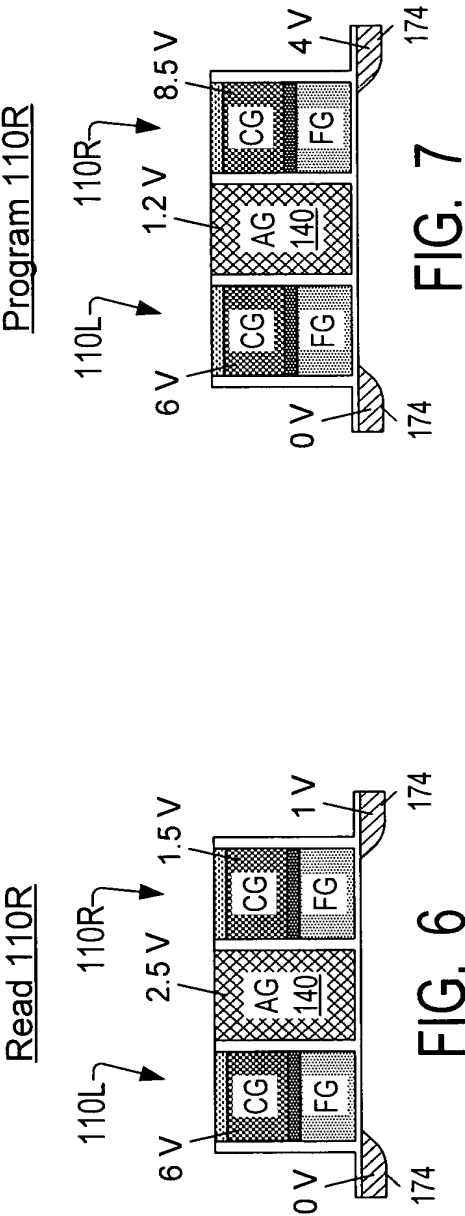
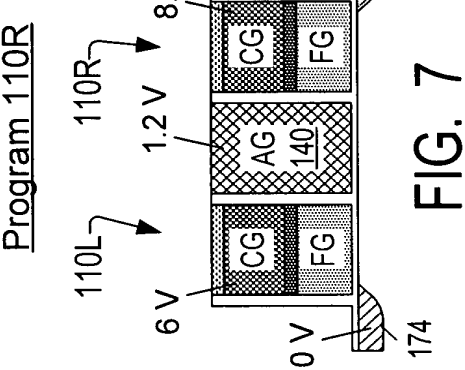


FIG. 5

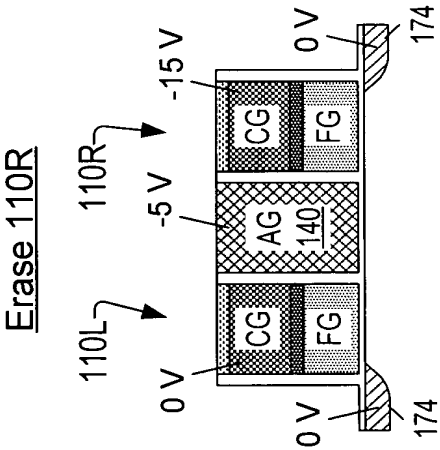
PRIOR ART



PRIOR ART



PRIOR ART



PRIOR ART

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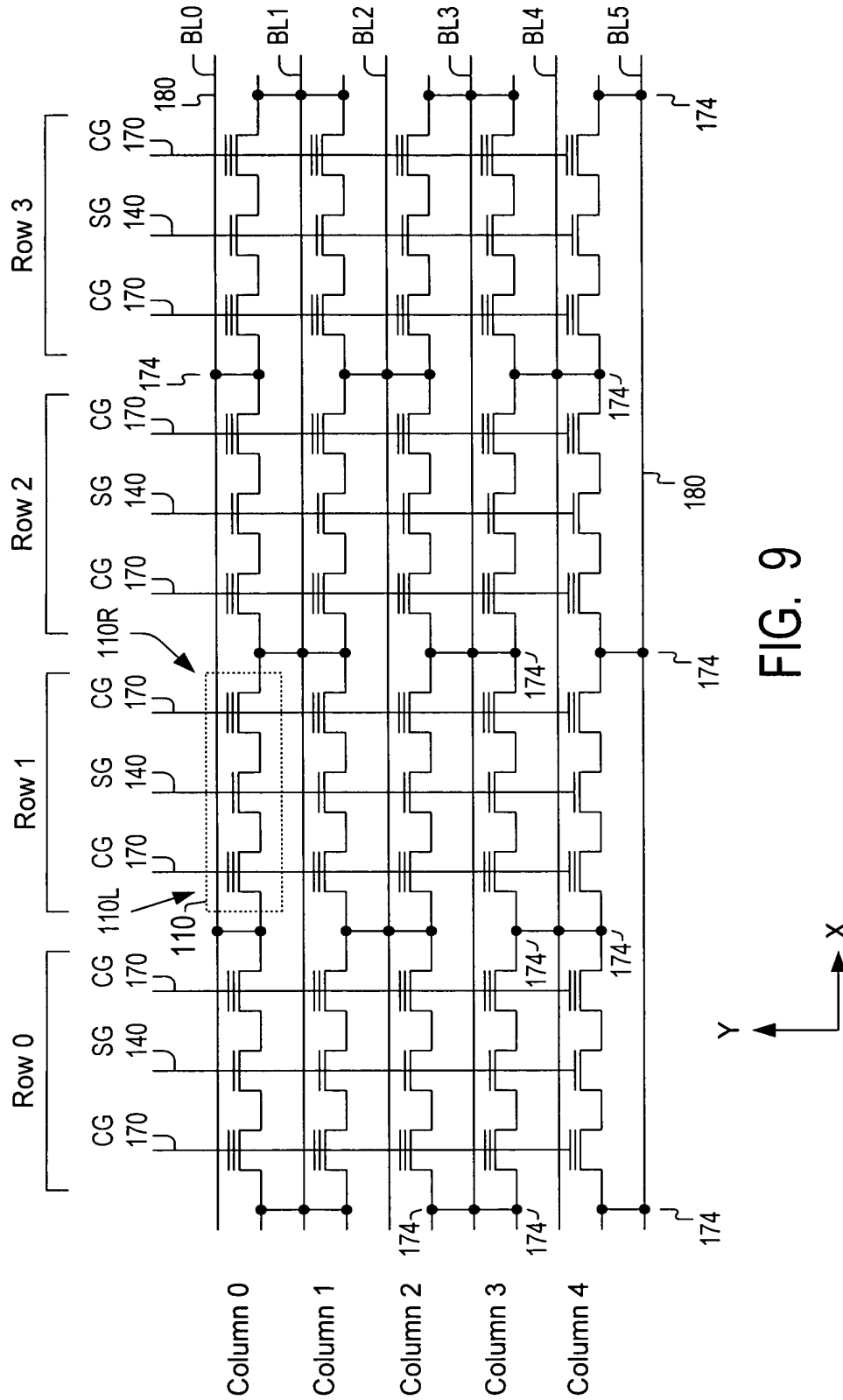


FIG. 9

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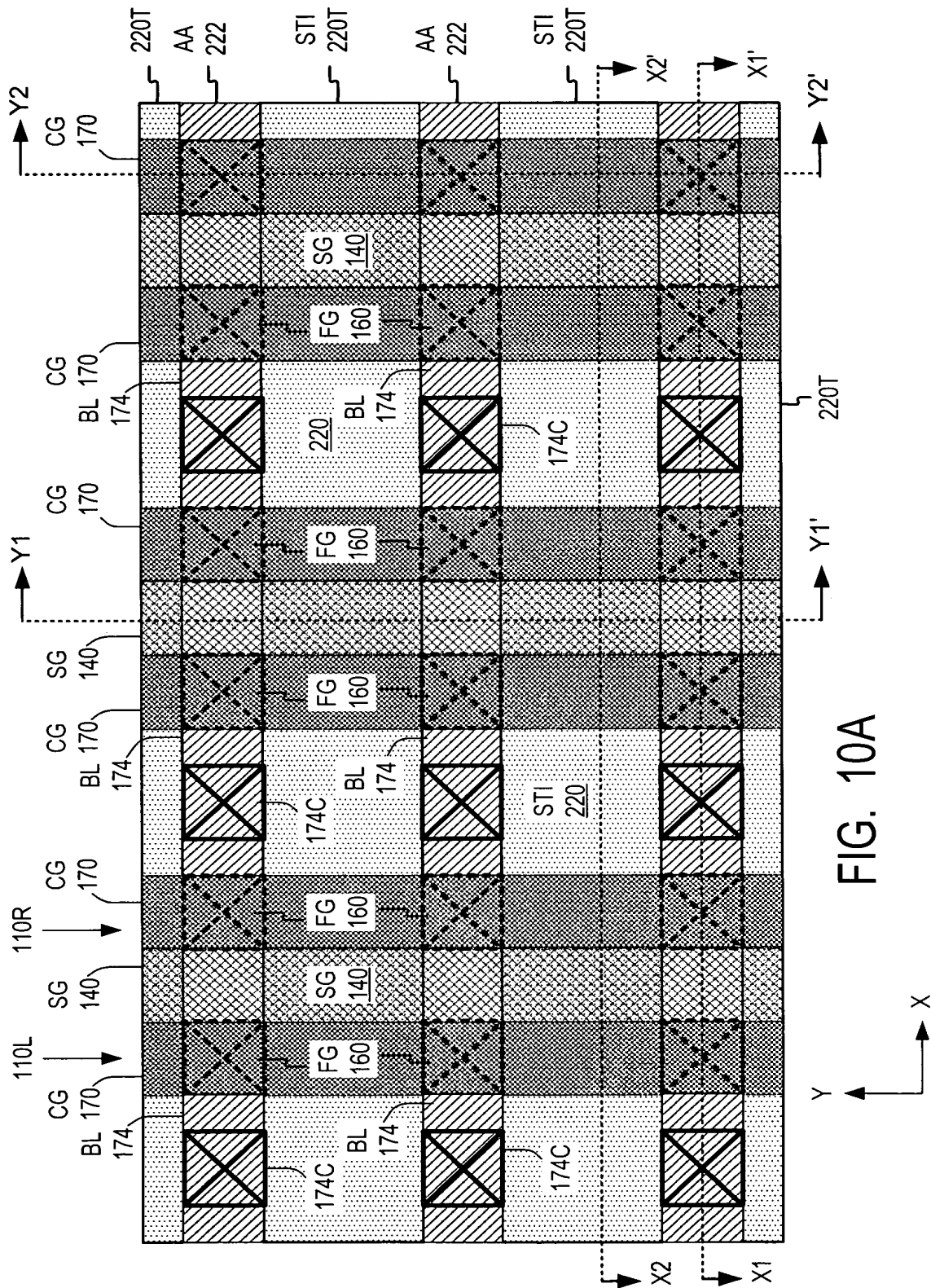
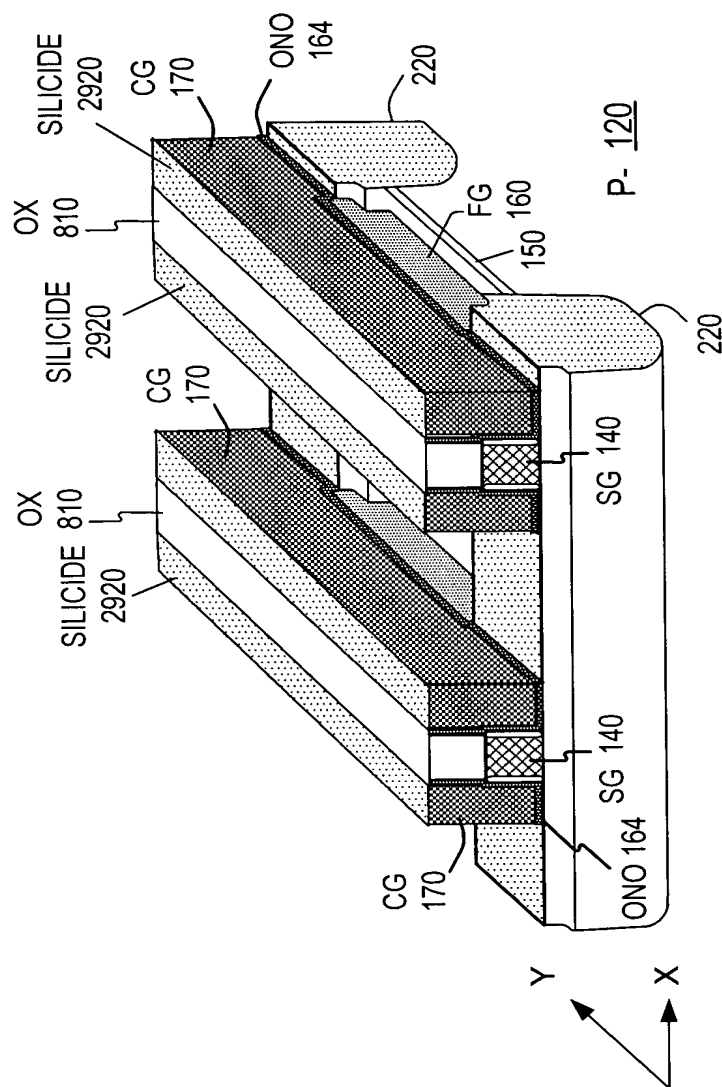


FIG. 10A



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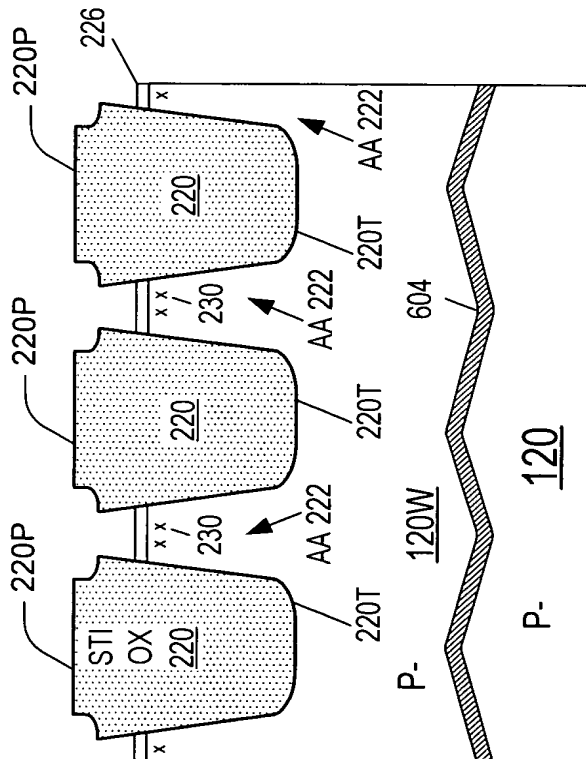


FIG. 11 (Y1-Y1'')

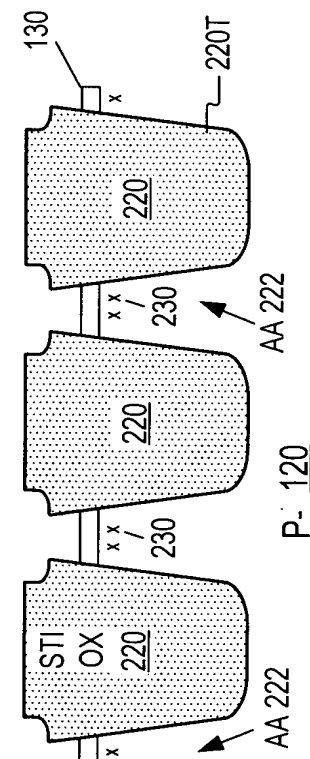


FIG. 12A (Y1-Y1')

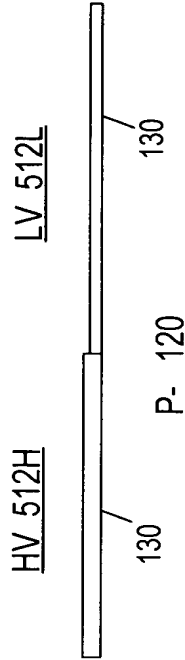


FIG. 12B
(PERIPHERY)

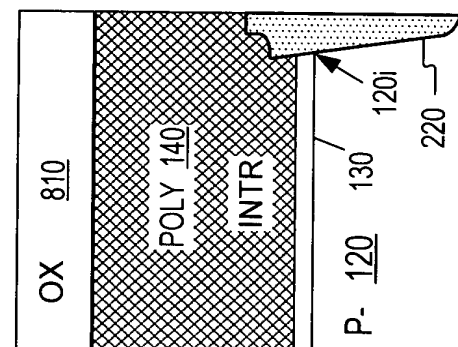


FIG. 13B
(PERIPHERY)

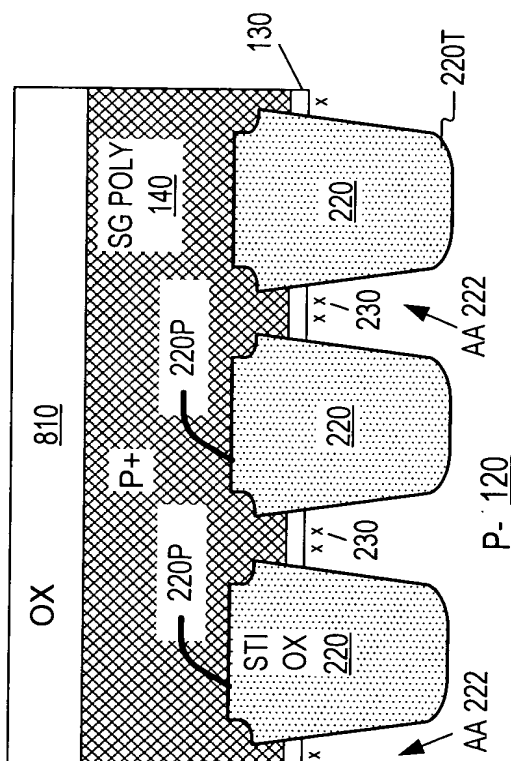


FIG. 13A (Y1-Y1')

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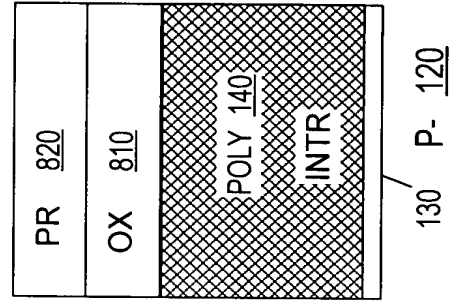


FIG. 14B
(PERIPHERY)

FIG. 15

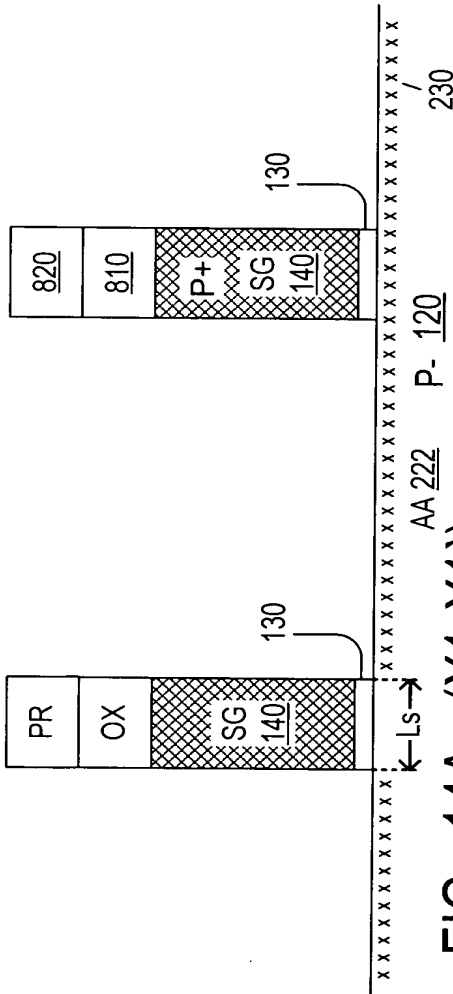
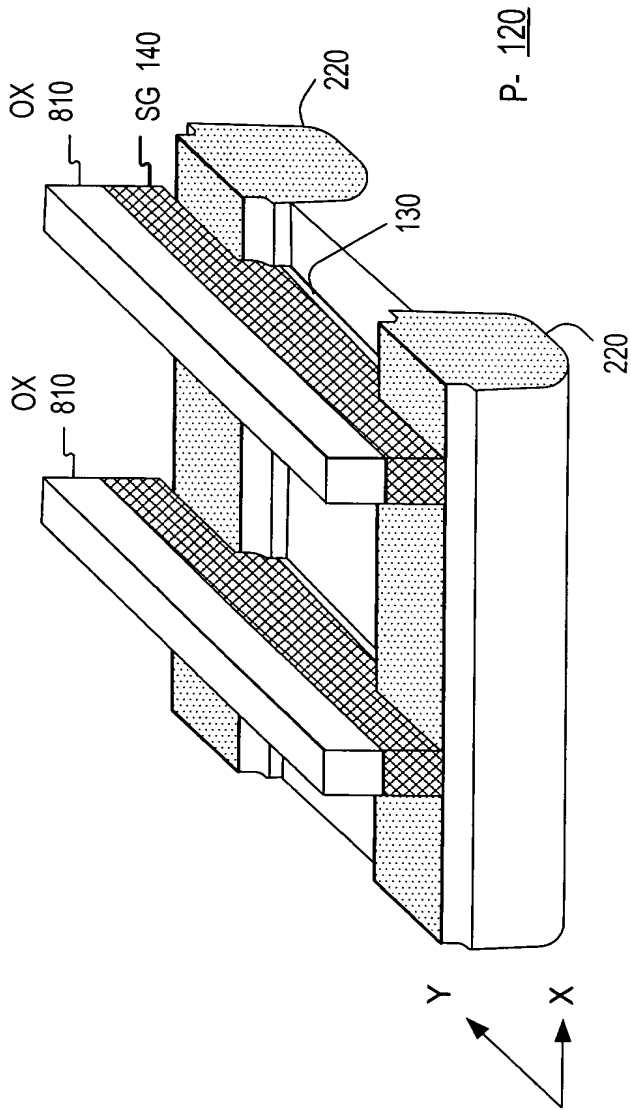
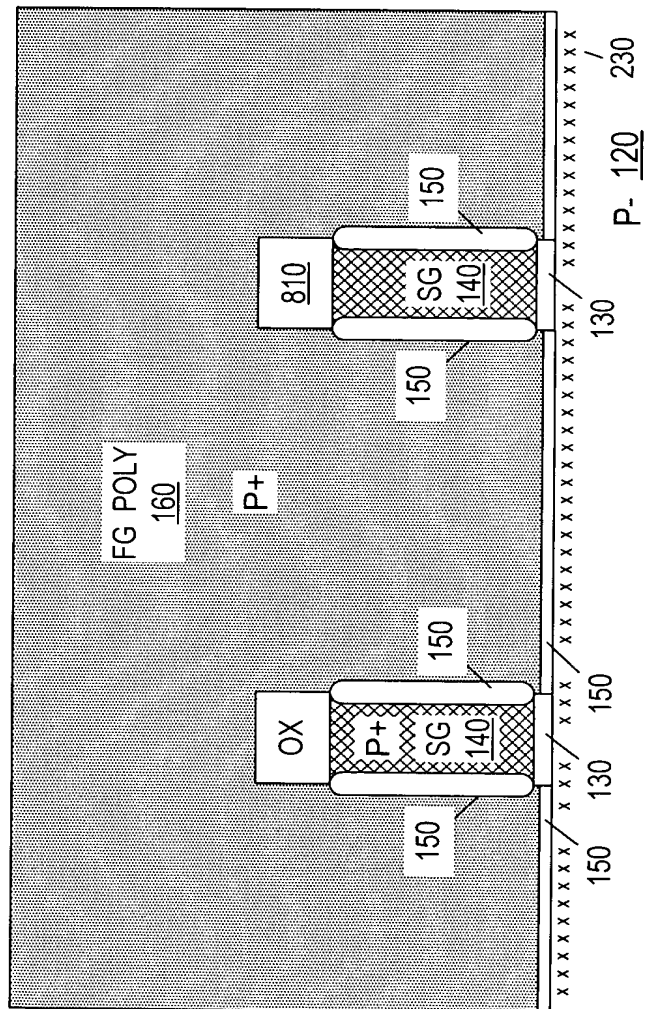
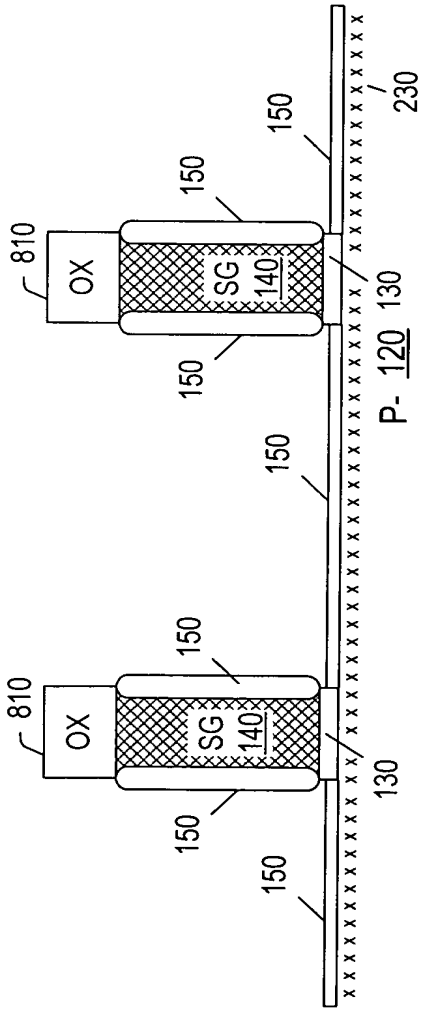


FIG. 14A (X1-X1')



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FIG. 18
(X1-X1')

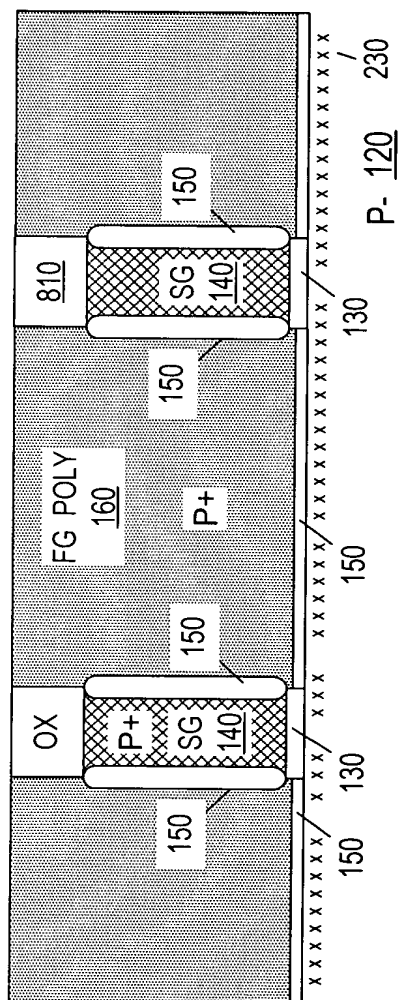


FIG. 19A
(X1-X1')

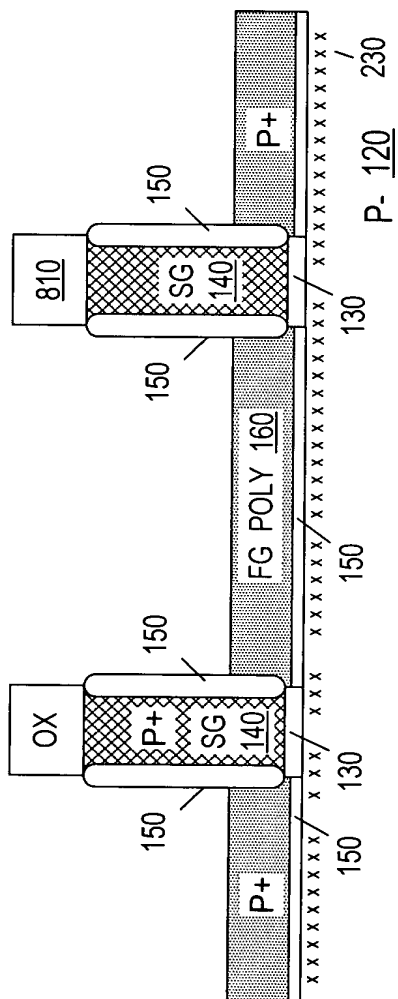
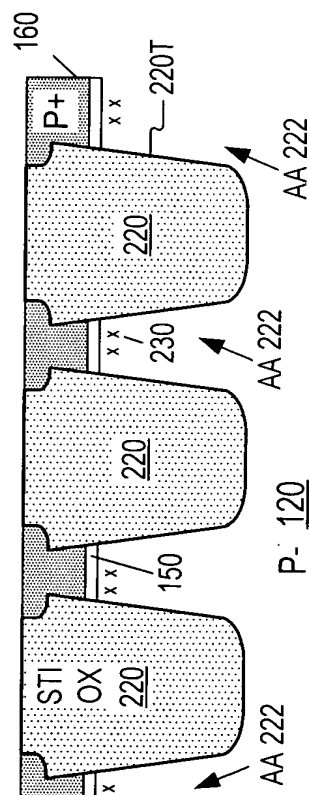


FIG. 19B
(Y2-Y2')



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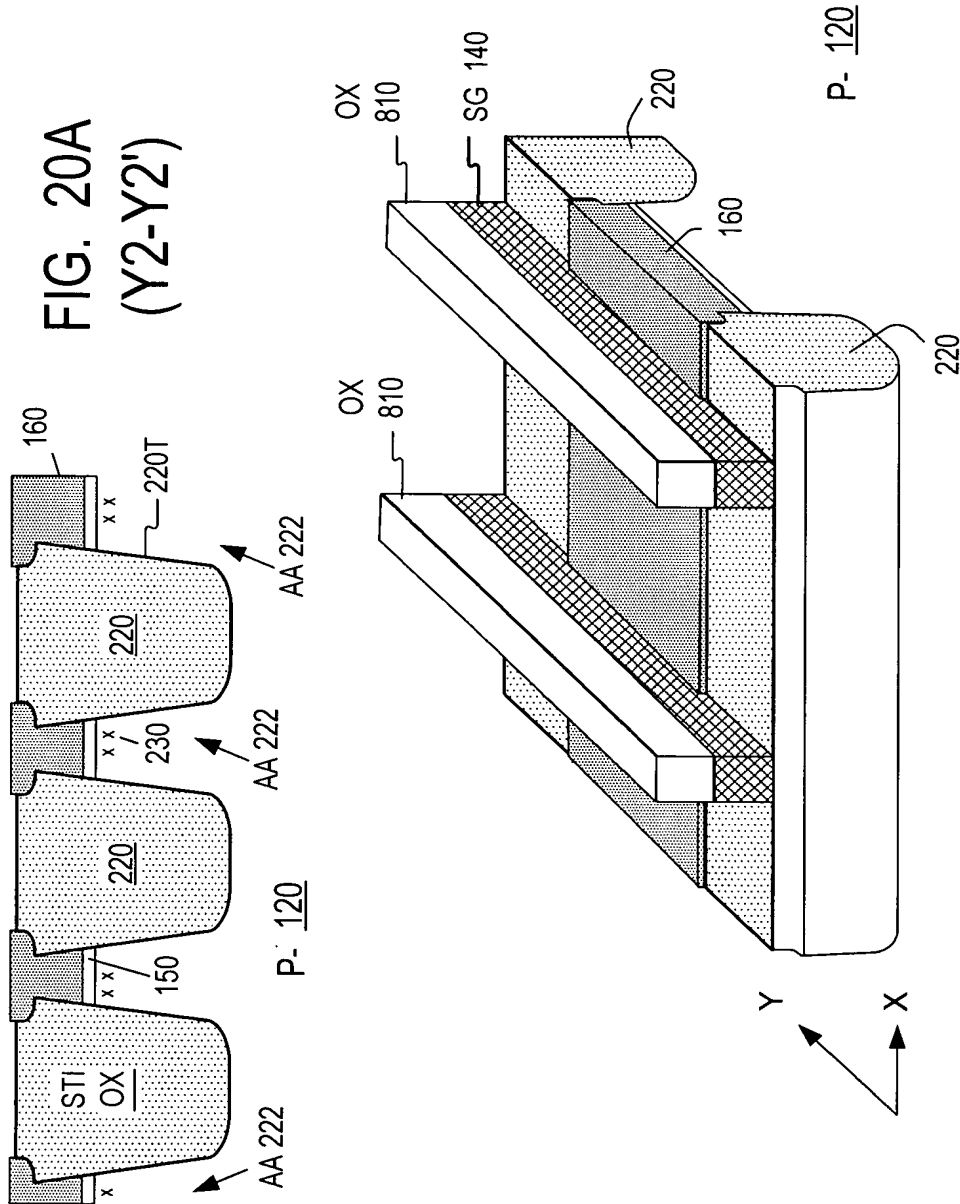


Figure 1 is a cross-sectional view of a semiconductor device. The device is divided into a peripheral region on the left and a central region on the right. The peripheral region includes a substrate 170C, a layer 170.1, a layer 170, a layer 130, a layer 120, a layer 110, a layer 810, a layer 164, and a layer 160. The central region includes a substrate 170C, a layer 170.1, a layer 170, a layer 130, a layer 120, a layer 110, a layer 810, a layer 164, and a layer 160. The central region also includes a gate stack (140) and a source/drain region (140).

FIG. 21A (X1-X1')

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FIG. 22
(X1-X1')

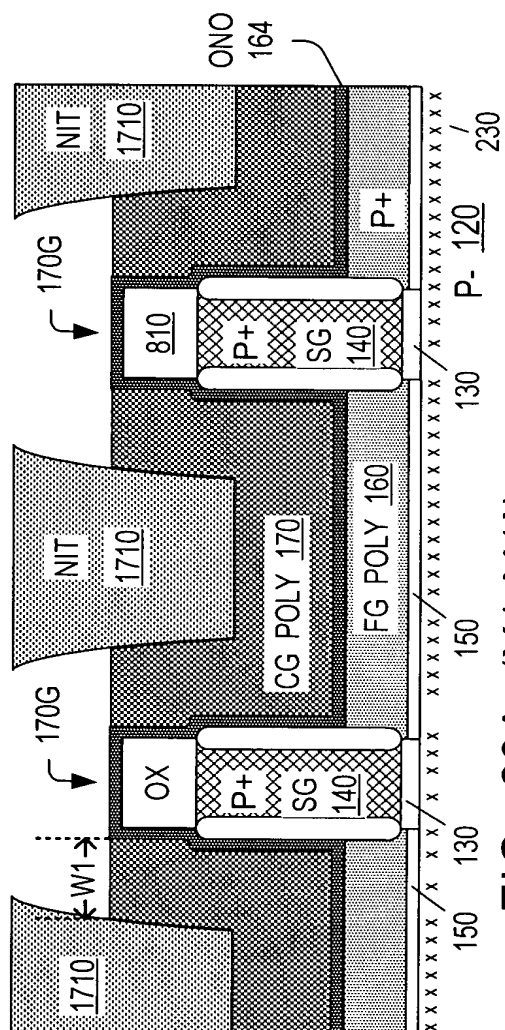
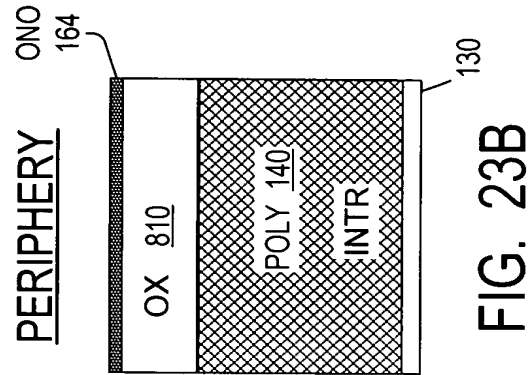
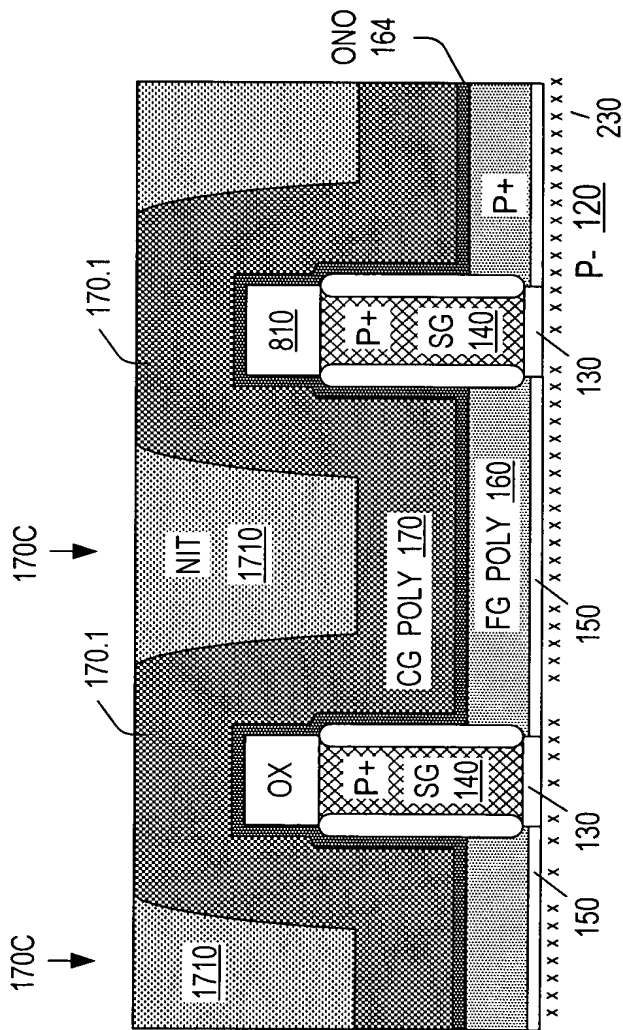


FIG. 23A (X1-X1')

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FIG. 24
(X1-X1')

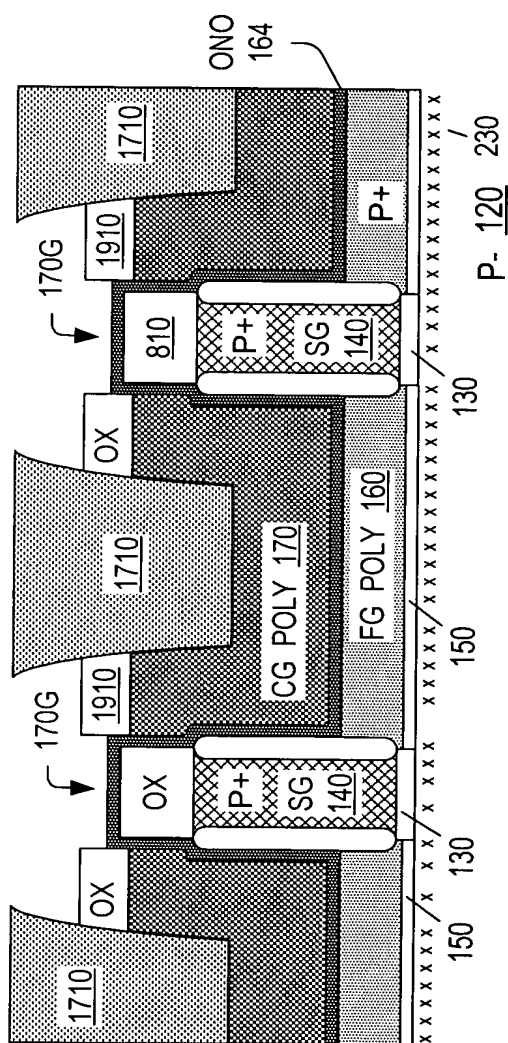
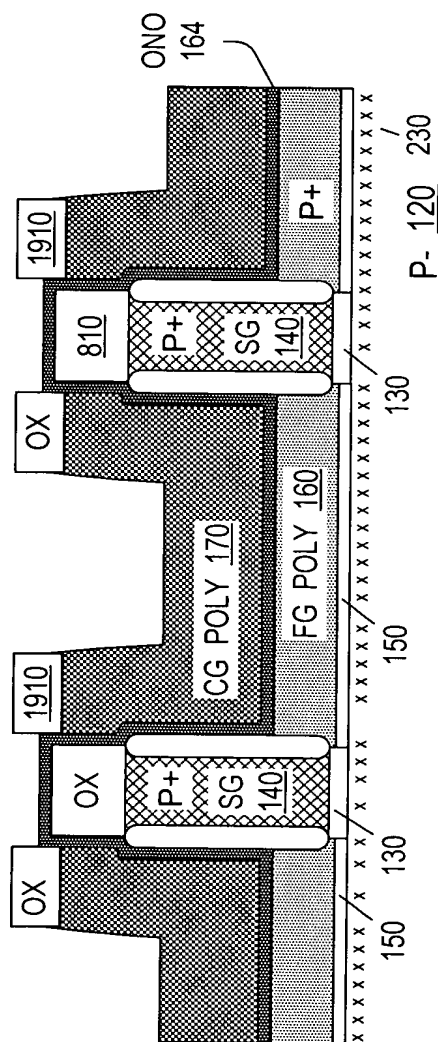


FIG. 25
(X1-X1')



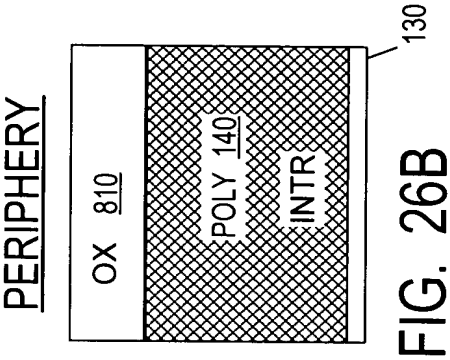
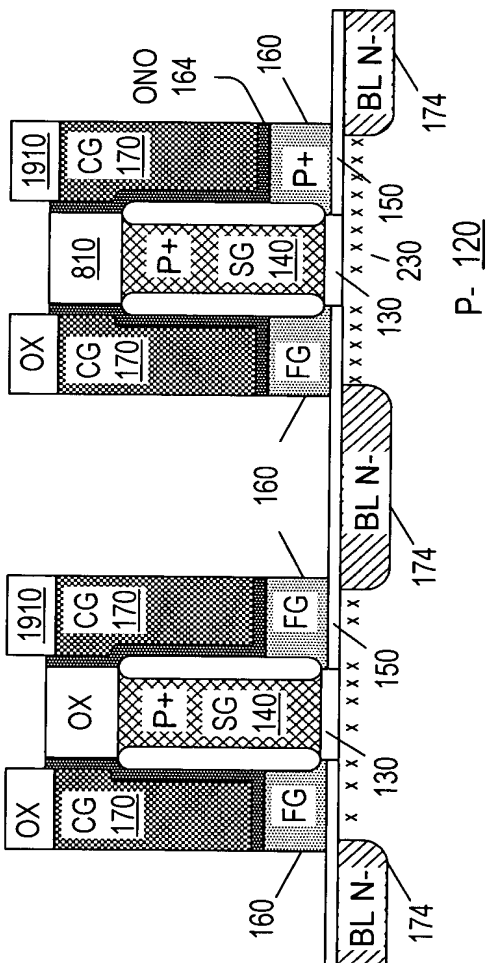
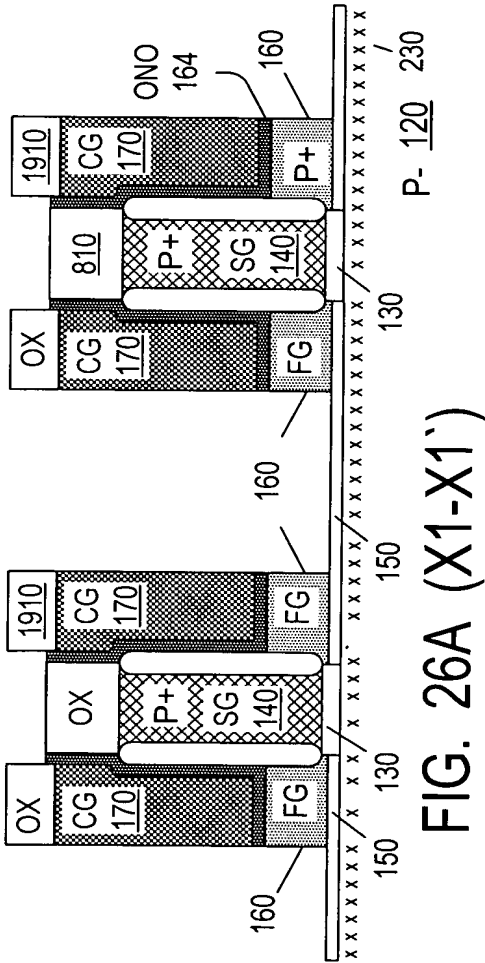
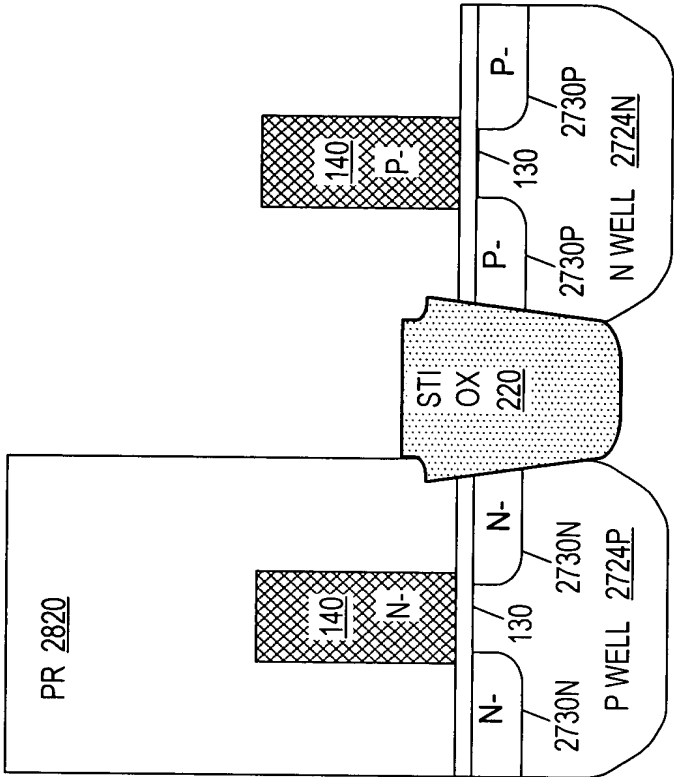


FIG. 27A
(X1-X1')



NMOS 512N

PMOS 512P

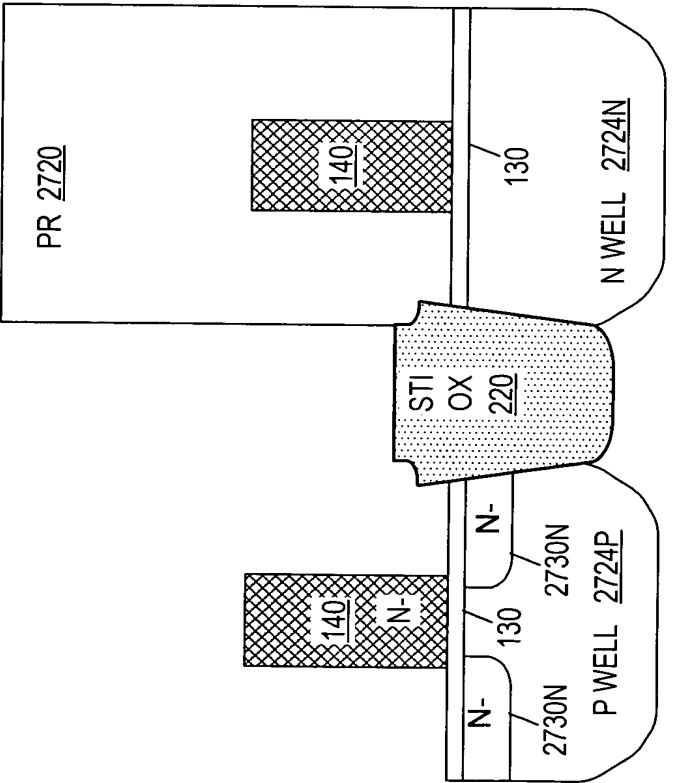


P- 120

FIG. 28
(PERIPHERY)

NMOS 512N

PMOS 512P



P- 120

FIG. 27B
(PERIPHERY)

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FIG. 29A
(X1-X1')

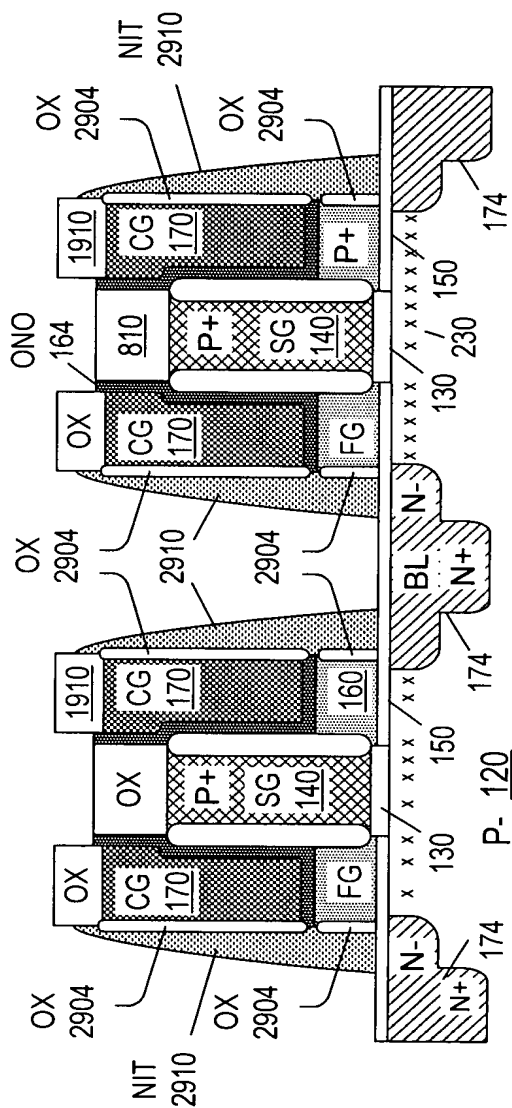


FIG. 29B
(PERIPHERY)

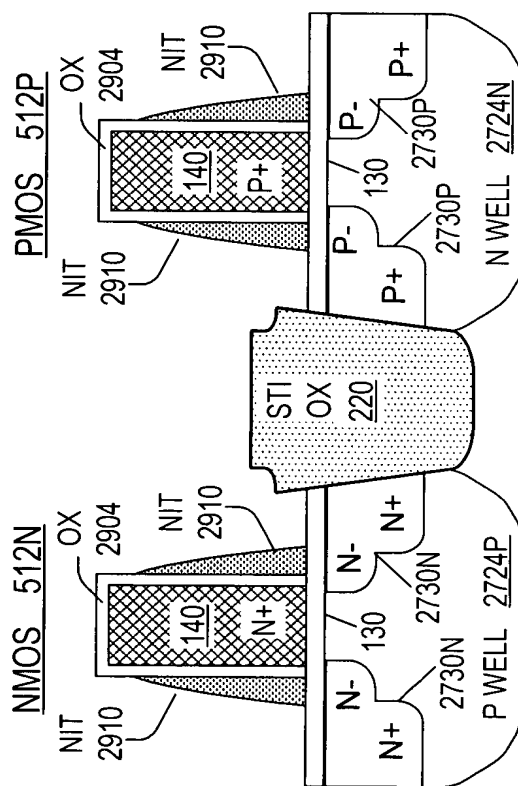


FIG. 30A
(X1-X1')

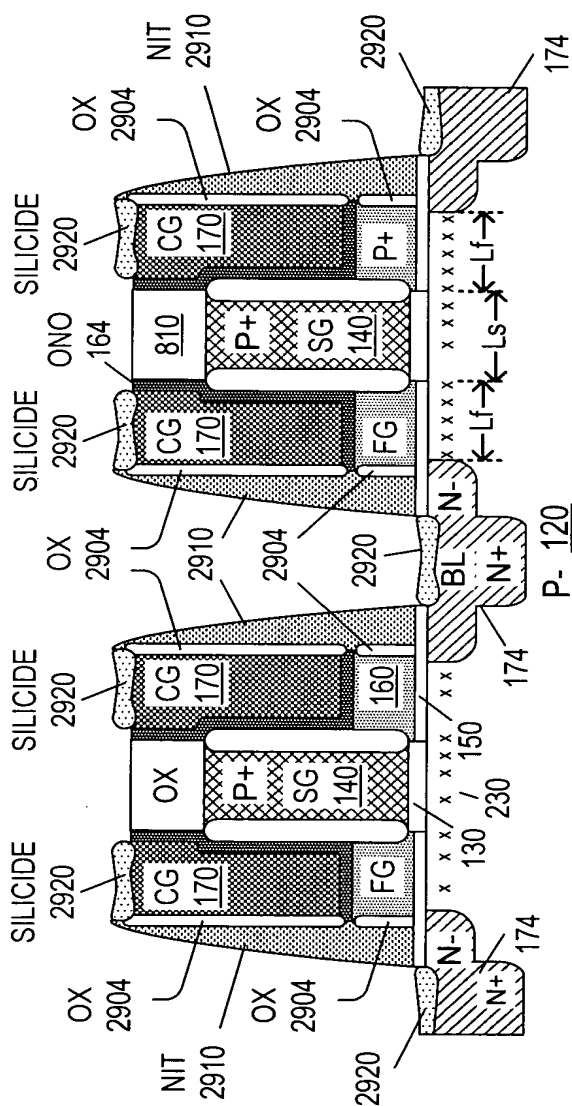
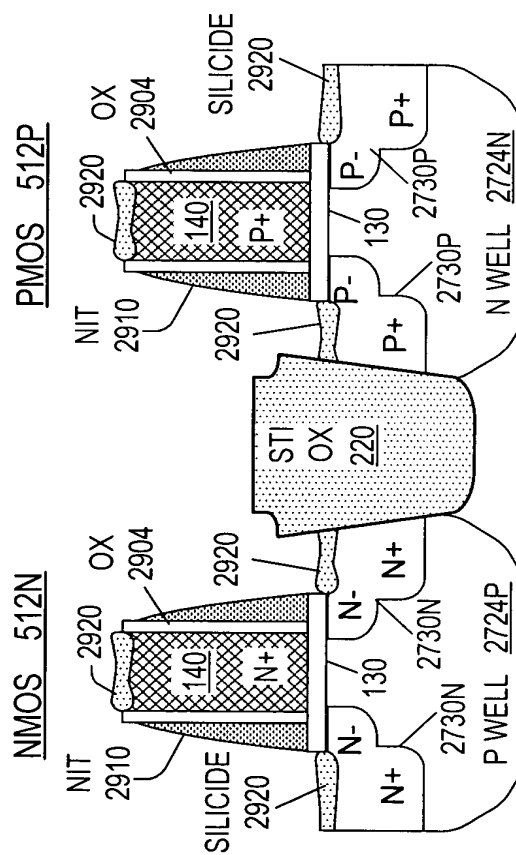


FIG. 30B
(PERIPHERY)



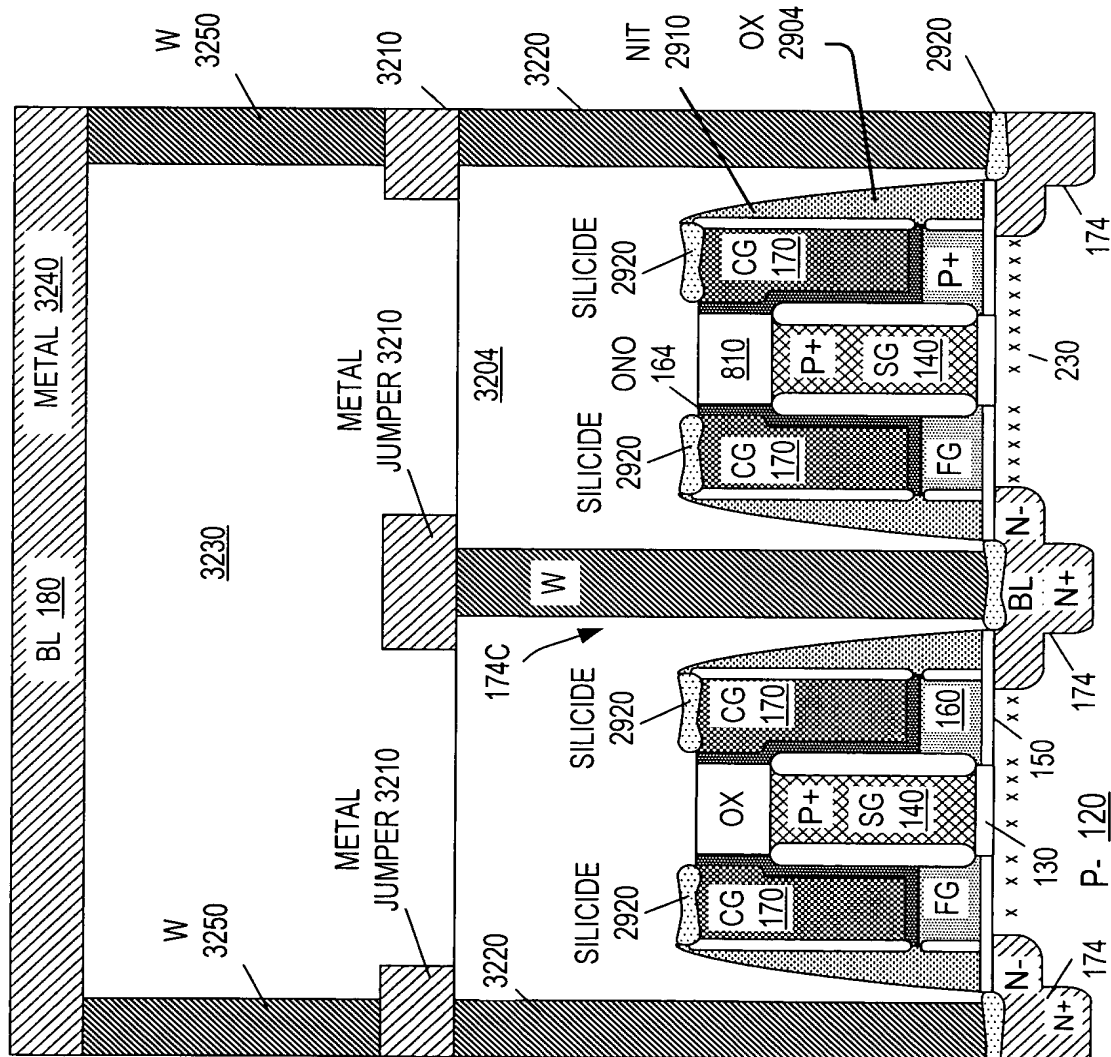


FIG. 31A (X1-X1')

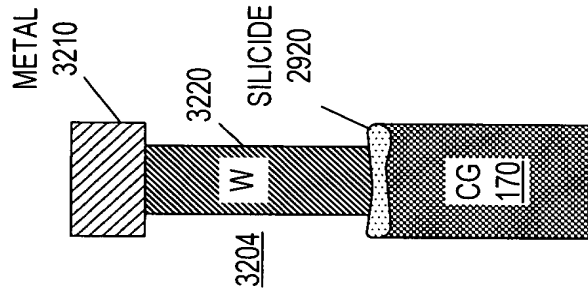


FIG. 31B
(ARRAY GAP OR
BOUNDARY)

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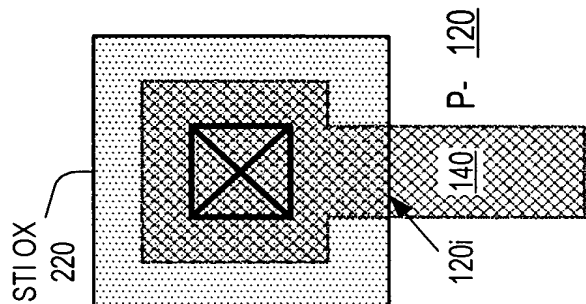


FIG. 31E
(PERIPHERY)

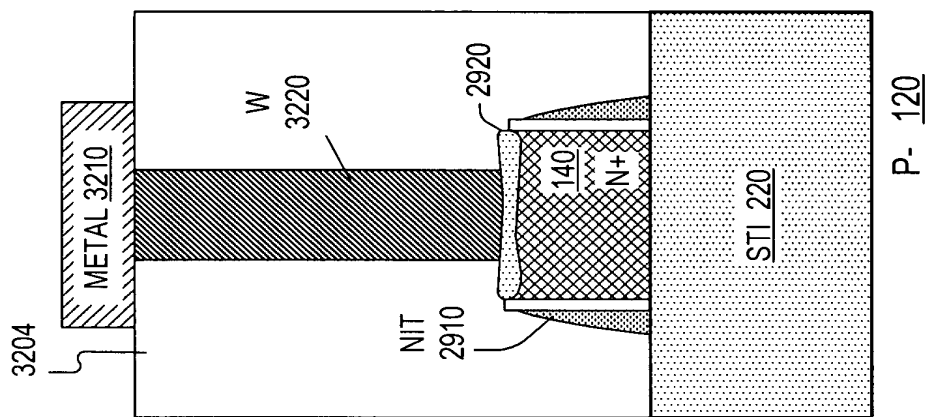


FIG. 31D
(PERIPHERY)

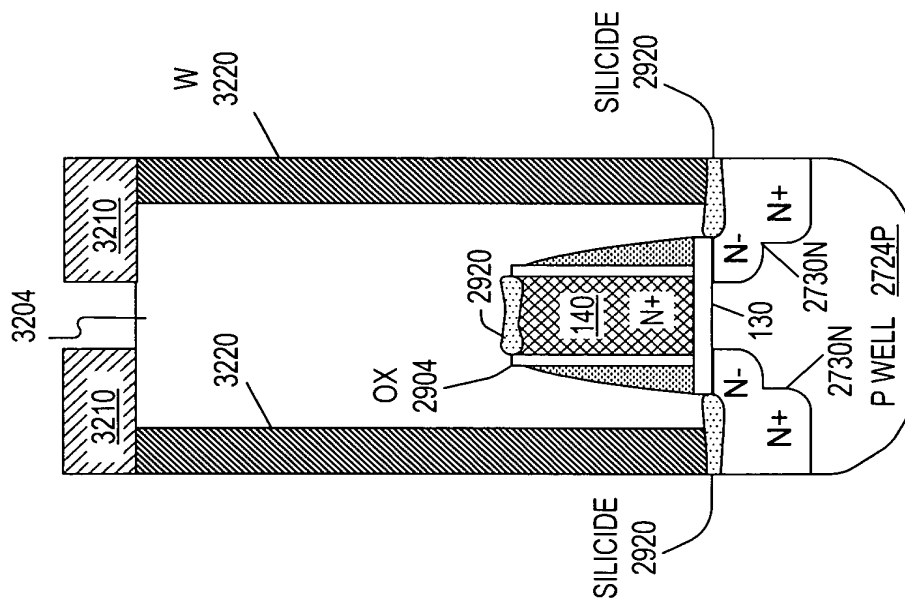


FIG. 31C
(PERIPHERY)

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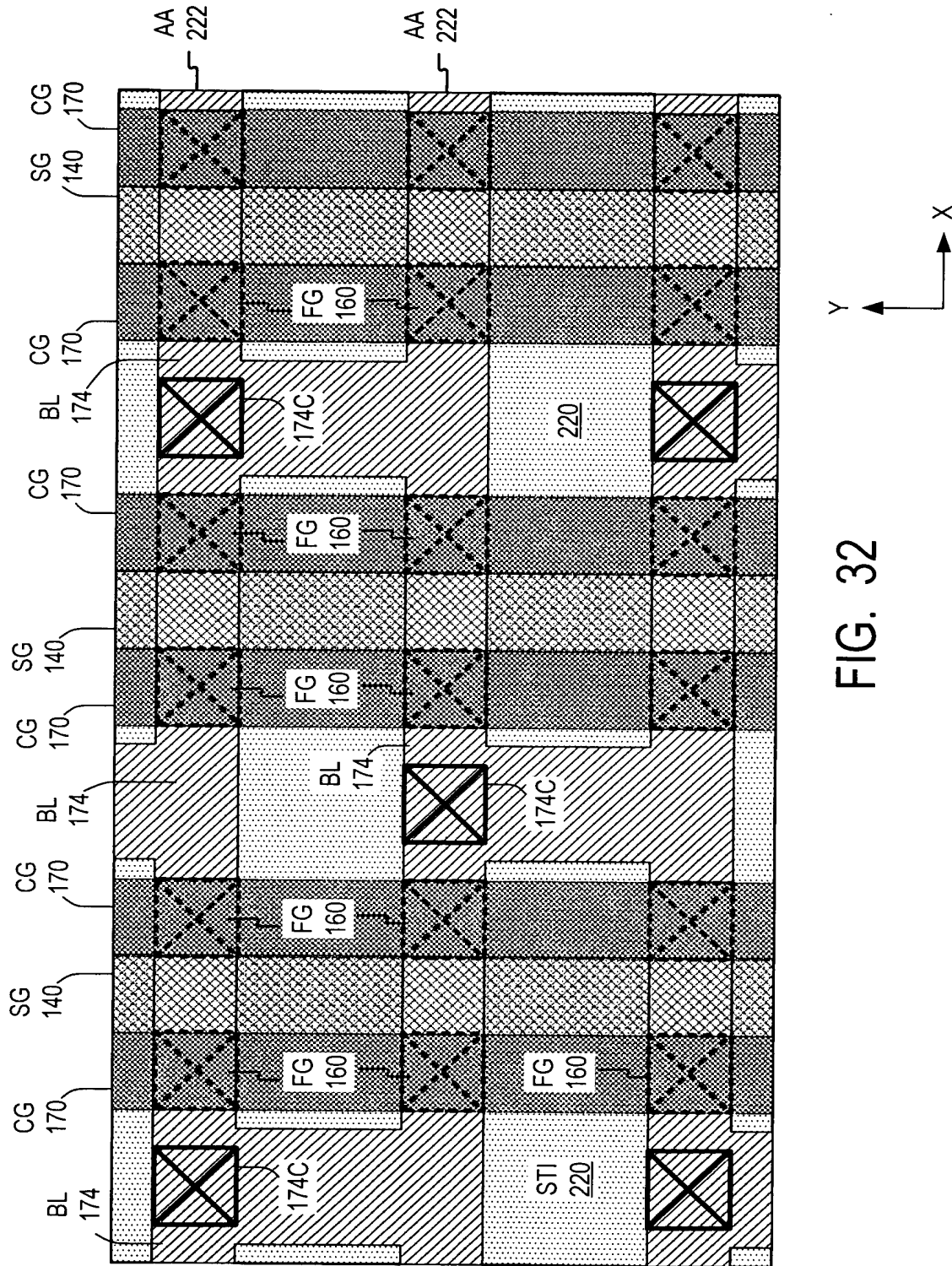


FIG. 32